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Analysis of Key Performance Parameters of Phase Sampling Digital RF Memories

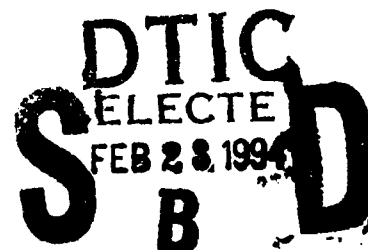
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13. ABSTRACT (Maximum 200 words) This report explores several performance features of phase sampling digital RF memories, starting with the phase sampling process itself. Spurious signal levels, bandwidth, and processing of simultaneous signals are analyzed using computer modeling of DRFM functions. The preferred phase sampling technique is to make phase comparisons between samples of the input signal and its 180° analog. The input amplifier and the noise immunity of the phase comparator determine the dynamic range. Theoretical spurious levels are tabulated for 2-, 4-, 8-, and 16-state sampling. The data reveal no differences between two-state and four-state sampling. Other tables show output levels for simultaneous signals into eight-state and two-state DRFMS at different combinations of input amplitudes. The advantages of the phase DFRM are large bandwidth, large input signal dynamic range without automatic gain control, and the capability for direct output phase modulation.				
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ANALYSIS OF KEY PERFORMANCE PARAMETERS OF PHASE SAMPLING DIGITAL RF MEMORIES

OBJECTIVE

In recent years, a number of questions have arisen regarding performance requirements for digital RF memory units (DRFMUs). Spurious signal levels (spurs), bandwidth, and processing of simultaneous and continuous wave (CW) RF signals are parameters frequently used to specify a DRFMU. Values for these parameters depend on the application. For example, a radar simulation may require extremely low spurs while an electronic countermeasures (ECM) technique may require maximum bandwidth. Of the three types of DRFMUs (amplitude sampling, Cartesian sampling, and phase sampling), phase DRFMUs are perhaps the least understood. The purpose of this report is to describe phase sampling DRFMUs (phase DRFMUs) and examine their performance. This work was sponsored by the Office of Naval Technology, Arlington, VA. Details on requirements for specific applications are addressed in a classified NRL report, "ECM Applications of Phase Sampling Digital RF Memories," to be published.

THE PHASE SAMPLING PROCESS

The phase sampling procedure is probably the most misunderstood aspect of the phase DRFMU. Oddly enough, phase sampling is the key trait that truly distinguishes this type of DRFMU from amplitude and Cartesian DRFMUs. A common misconception is that the amplitude of the incoming waveform is compared to different voltage amplitudes, converted to a phase value, and stored. This scheme requires automatic gain control (AGC) to maintain a fixed amplitude with minimum signal distortion (no limiting of the signal). A fixed amplitude is needed when measuring intermediate phase values, such as $\pi/4$ or $\pi/8$. This flawed approach exhibits less dynamic range than do phase sampling techniques that do not require an AGC.

The preferred sampling technique is to generate a single digital code from 1-bit representations of different phase-shifted signals derived from the input signal. The generation of each 1-bit code is best accomplished by comparing each phase-shifted signal with its 180° counterpart. While this same effect could be obtained by comparing the phase-shifted signal to ground, use of the 180° analog comparison removes any ambiguity resulting from amplifier distortion or ground noise.

Figure 1 is an example of the sampling necessary for an eight-state DRFMU. Here, the phase of each signal sample is compared with its 180° component. The zones within the circles represent the phase of the input signal. A high output from a comparator puts the signal in zone A and a low output means the signal is in zone B. For example, the quadrature sample allows one to determine whether the phase of the input signal is between $\pi/2$ and $3\pi/2$ or between $3\pi/2$ and $\pi/2$ radians.

Figure 1 is a composite diagram showing how a set of comparisons can uniquely specify the phase of the input signal. Generally, to get a $2n$ (where $n = \{1, 2, \dots\}$) phase state, DRFMU requires n comparisons generating an n -bit Johnson code. However, $2n$ states can be independently coded with only $\text{int}[\log_2(2n)]$ bits, with fractions rounded to the next largest integer. Thus, the initial Johnson code for the states is compressed. For example, an eight-state DRFMU requires four comparisons resulting in a

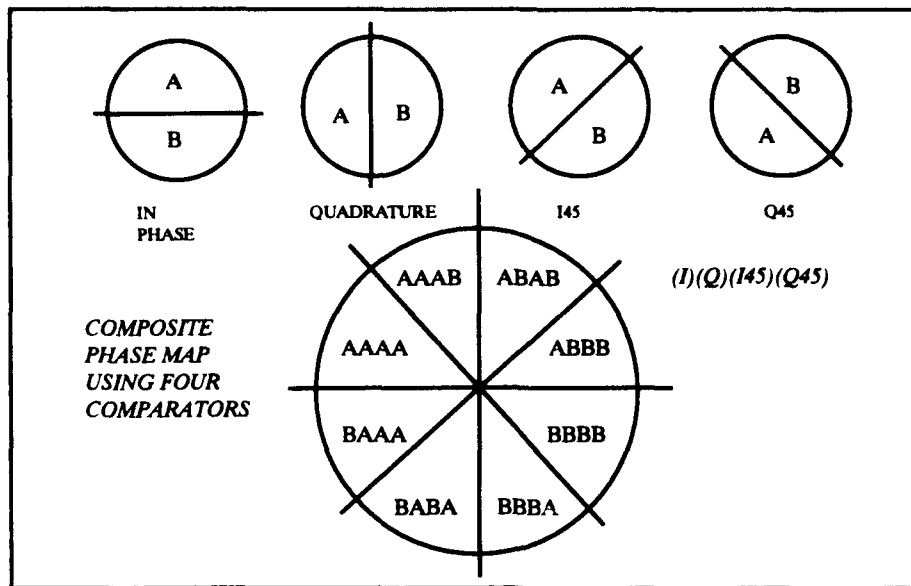


Fig. 1 — Phase comparisons for an eight-state DRFMU

four-bit Johnson code that can be compressed into a unique three-digit code for each of the eight states. This reduces the number of bits stored while not seriously affecting the maximum clock speed of the DRFMU. Three comparisons alone will not generate all eight codes. Two codes will recur. This becomes apparent if one tries to generate the eight states in Fig. 1 without using one of the four comparators. For those cases where the number of states is not a power of 2, the minimum number of bits is rounded to the next power of 2.

The compressed code must be uncompressed before recombination to recreate the signal. Anaren Microwave has developed an eight-state DRFMU that uses an elegant yet practical method for phase sampling, code compression and uncompression, and signal regeneration. Figures 2 and 3 show how the digital-to-phase and phase-to-digital DRFMUs operate.

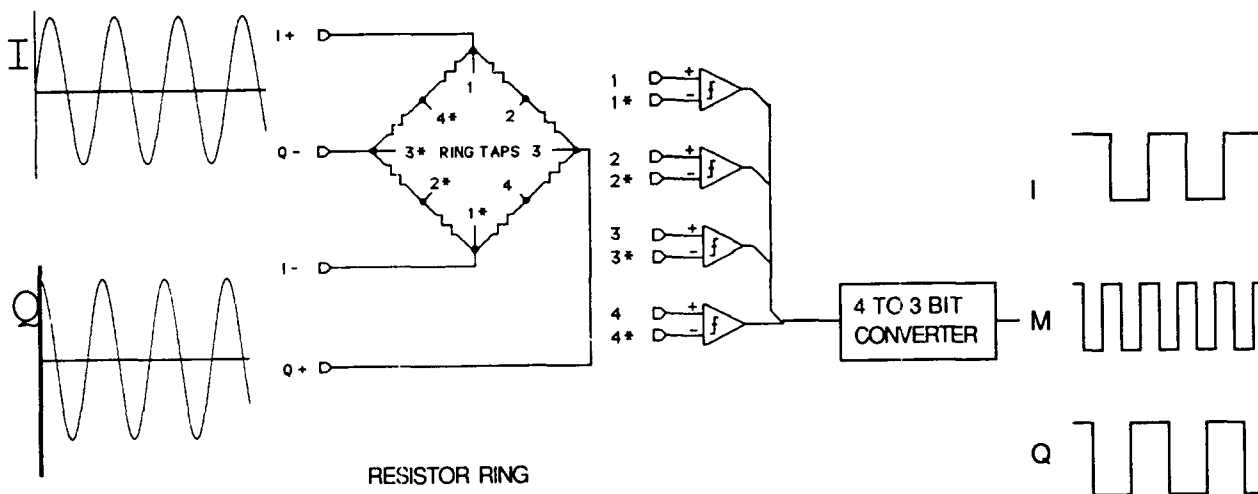


Fig. 2 — Anaren Microwave 3-bit phase-to-digital converter.
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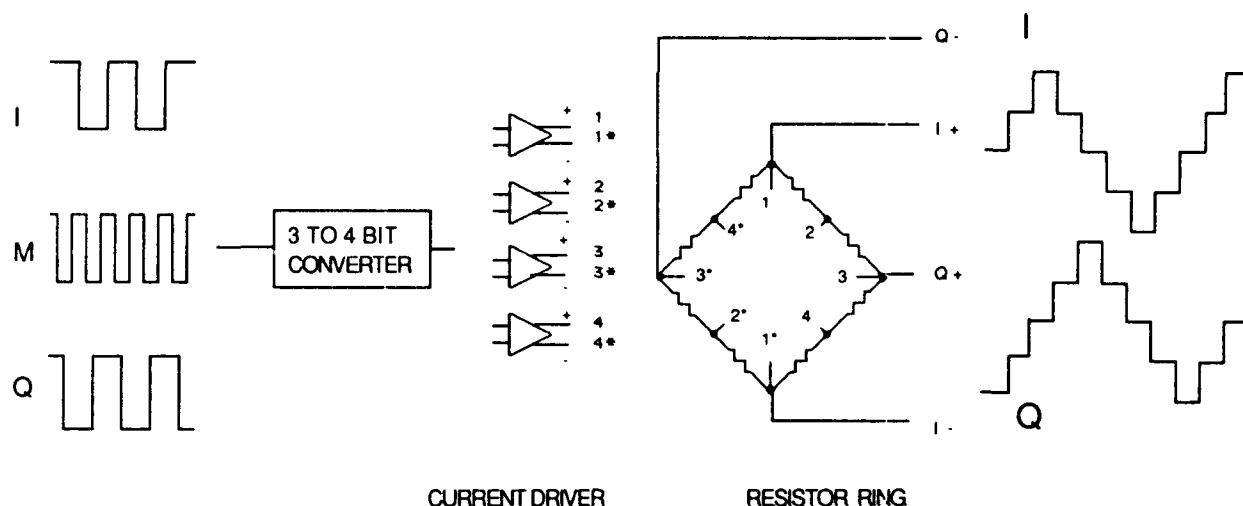


Fig. 3 — Anaren Microwave three-bit phase-to-digital converter.
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While it is not mandatory to use quadrature signals and equally spaced phase offsets, there are excellent reasons for doing so. First, quadrature signals are easily obtained from a quadrature mixer or a hybrid splitter (not shown). The other phases can be derived from I , Q , I' , and Q' . A symmetrical resistor ring in Fig. 2 derives these other phases, while the ring in Fig. 3 recombines the phases. Second, a quadrature mixer in up and down conversion preserves the direction of phase rotation and allows storage of signals on either side of the local oscillator (LO). This effectively doubles the bandwidth of the device. Third, equally partitioning the phase zones improves the spurious performance of the output signal.

DYNAMIC RANGE

The previous discussion on phase sampling did not establish the power requirements for the input signal or the dynamic range of the DRFMU. The input amplifier and the noise immunity of the comparator determine the dynamic range. The comparator needs some margin above noise for determining which of two signals is larger, and this sets the minimum input signal level. If this margin is made too small, then noise will trigger changes in the comparator output, and corrupted data will be stored.

The type and power capabilities of the input amplifier set the maximum input signal. In fact, a limiting amplifier can be used since this type of DRFMU preserves only phase information. Therefore, the noise floor of the operating environment is the theoretical limit on the dynamic range of the phase DRFMU. The output signal integrity and spurious response are less sensitive to the input signal level. This is a major difference between phase and amplitude DRFMUs.

SPURIOUS SIGNALS

The spurious performance of a phase DRFMU can be defined in a number of ways. Some examples are

- the maximum spur level that occurs in the entire operating frequency band,
- the average value of the maximum spur level across the operating bandwidth, and
- the average total spurious power over the operating bandwidth.

Any of these performance levels would be difficult to calculate theoretically. A rigorous solution would require analytical expressions for the spurs of a sampled quantized waveform. This is far beyond the scope of this report. However, it is possible to derive intuitively the type of performance that can be expected by examining a few frequencies in detail. Harmonic levels can be calculated, but they do not portray a complete spurious response.

Figure 4 illustrates a method for determining the spurious response of the phase DRFMU. This scheme generates the phase as a function of the sampling clock frequency. This generalizes the results to make them independent of the actual clock frequency. Next, the model quantizes the phase to the appropriate number of bits. It replicates each signal sample four times for increased resolution. This does not introduce any error in quantized waveforms, but is important when interpreting the actual frequencies of the resulting fast Fourier transform (FFT). All calculations assume a perfect anti-aliasing filter, i.e., they do not use any frequency above one half the clock frequency. Since all frequencies below the LO have spurious performance mirrored by frequencies above the LO, only positive frequencies were considered.

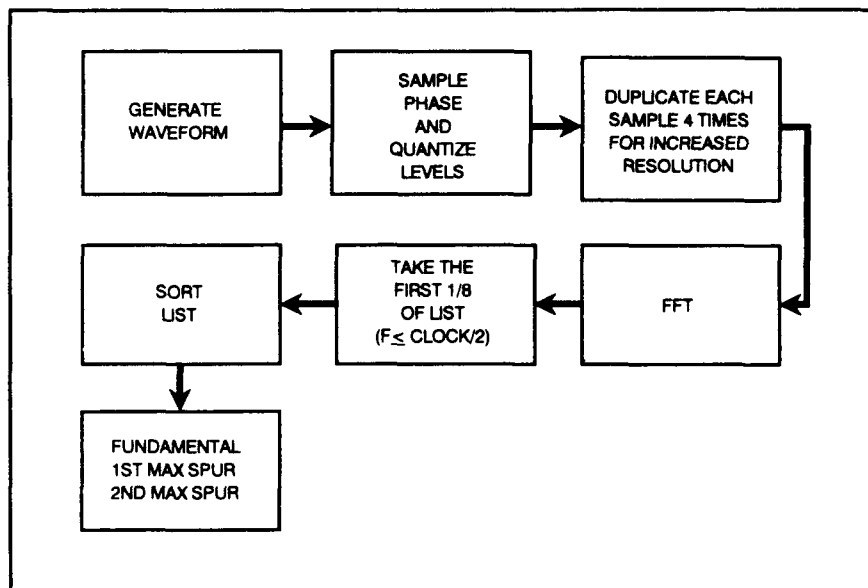


Fig. 4 — Model for calculating DRFMU spurious response

The model reconstructs the waveform by assigning an amplitude to each phase (n phase states convert to $(n/2)+1$ amplitudes) that could be weighted. Nonweighted reconstruction increments or decrements the amplitude between any two phase zones equally. A weighted scheme changes the amplitude in proportion to the amplitude change between the same two phases on a sinusoid. For example, at $\pi/6$ and $\pi/4$, the normalized weighted amplitudes are 0.5 and 0.707, respectively, whereas using unweighted values, $\pi/4$ would be 0.5. For practical systems, the improved spurious performance that is achieved does not usually justify the increase in complexity of a weighted system.

Tables 1 through 5 summarize the results. The tables contain calculated values for the three highest spurs at discrete frequencies across the band. Tables 1 through 4 are results for 2, 4, 8, and 16-state DRFMUs. Table 5 is for a weighted 16-state unit. Operating frequencies are given as fractions of the clock frequency. For example, if the clock is 1000 MHz, 1/4 in the table is 250 MHz RF input. The spur levels shown are in decibels referenced to the fundamental power. The fundamental power is expressed in decibels relative to a pure sine wave of the same peak amplitude. The power drop with increasing frequency is characteristic of phase DRFMUs. A limiting amplifier in the output stage

Table 1 — Two-state Spurious Response

Frequency Relative to Clock	Power at Fundamental Frequency	Spurious Peaks, dBc		
		1st	2nd	3rd
1/16	2.1	-9.5	-13.9	-16.7
3/32	2.0	-10.4	-16.7	-17.8
1/8	2.1	-9.4	—	—
5/32	1.8	-12.3	-14	-16
3/16	1.7	-11.4	-12.2	-14.9
7/32	1.5	-10.4	-13.1	-17.3
1/4	2.2	—	—	—
9/32	1.0	-8.7	-14.9	-15.1
5/16	0.8	-7.8	-13.1	-14
11/32	0.4	-7.8	-13.1	-16.4
3/8	0.3	-5.9	—	—
13/32	-0.2	-7.7	-11.3	-14.2
7/16	-0.6	-7.7	-10.3	-11.3
15/32	-1.1	-8.6	-12.1	-14.1

—No spurs present

Table 2 — Four-state Spurious Response

Frequency Relative to Clock	Power at Fundamental Frequency	Spurious Peaks, dBc		
		1st	2nd	3rd
1/16	-0.5	-9.5	-13.9	-16.7
3/32	-0.5	-10.4	-16.7	-17.8
1/8	-0.5	-9.4	—	—
5/32	-0.6	-12.3	-14	-16
3/16	-0.7	-11.3	-12.2	-14.9
7/32	-0.8	-10.4	-13.1	-17.3
1/4	-0.4	—	—	—
9/32	-1.0	-8.7	-14.9	-15.1
5/16	-1.1	-7.8	-13.1	-14
11/32	-1.3	-7.8	-13.1	-16.4
3/8	-1.3	-5.9	—	—
13/32	-1.6	-7.7	-11.3	-14.2
7/16	-1.8	-7.7	-10.3	-11.3
15/32	-2.1	-8.6	-12.1	-14.1

Table 3 — Eight-state Spurious Response

Frequency Relative to Clock	Power at Fundamental Frequency	Spurious Peaks, dBc		
		1st	2nd	3rd
1/16	-0.8	-16.7	-17.2	-21.5
3/32	-0.9	-17.8	-18.1	-22.4
1/8	-0.8	-17.1	—	—
5/32	-1.0	-16	-20	-20
3/16	-1.0	-14.9	-19	-19.8
7/32	-1.1	-17.3	-18.1	-18.8
1/4	-0.4	—	—	—
9/32	-1.3	-15.1	-16.3	-19.7
5/16	-1.5	-13.1	-15.4	-21.6
11/32	-1.6	-15.4	-16.4	-16.9
3/8	-1.7	-13.5	—	—
13/32	-2.0	-14.2	-15.4	-17.2
7/16	-2.1	-11.3	-15.3	-18
15/32	-2.4	-14.1	-15.4	-16.2

Table 4 — Sixteen-state Spurious Response

Frequency Relative to Clock	Power at Fundamental Frequency	Spurious Peaks, dBc		
		1st	2nd	3rd
1/16	-0.9	-18.6	-26.5	-30.8
3/32	-0.9	-19.5	-22.4	-29.3
1/8	-1.1	-24.7	—	—
5/32	-1.0	-21.4	-21.5	-26.6
3/16	-1.1	-20.5	-24.8	-28.9
7/32	-1.2	-19.5	-20.6	-25.7
1/4	-1.5	—	—	—
9/32	-1.4	-17.8	-19.7	-27.5
5/16	-1.5	-16.9	-26.6	-27.2
11/32	-1.7	-16.9	-18.8	-25.7
3/8	-2.0	-21.2	—	—
13/32	-2.2	-16.8	-17.9	-23.9
7/16	-2.2	-16.8	-22.9	-25.3
15/32	-2.5	-16.9	-17.7	-24.7

Table 5 – Sixteen-state Weighted Spurious Response

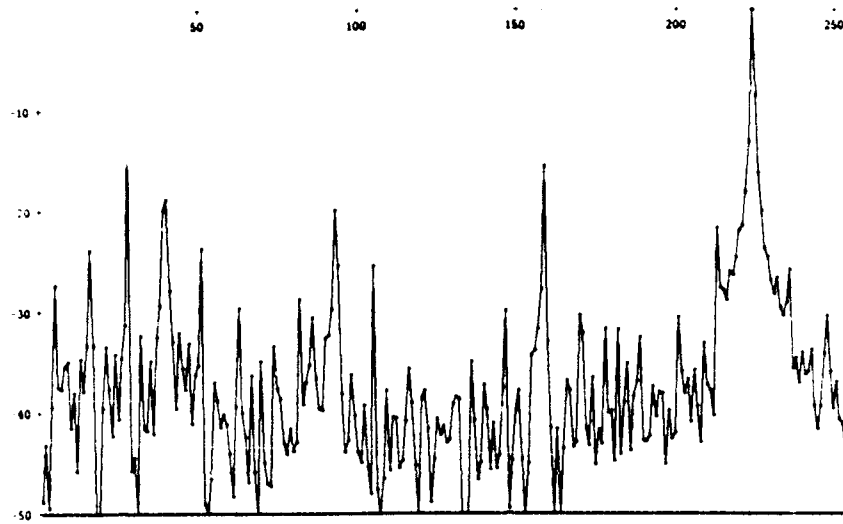
Frequency Relative to Clock	Power at Fundamental Frequency	Spurious Peaks, dBc		
		1st	2nd	3rd
1/16	-0.0	—	—	—
3/32	-0.1	-22.4	—	—
1/8	-0.1	—	—	—
5/32	-0.2	-21.5	—	—
3/16	-0.2	—	—	—
7/32	-0.4	-20.6	—	—
1/4	-0.4	—	—	—
9/32	-0.6	-19.7	—	—
5/16	-0.7	—	—	—
11/32	-0.9	-18.8	—	—
3/8	-1.0	—	—	—
13/32	-1.2	-17.9	—	—
7/16	-1.4	—	—	—
15/32	-1.6	-16.9	—	—

compensates for this power drop, and further reduces spur levels if the harmonics occur outside of the system bandwidth. The theoretical maximum harmonic within the bandwidth will be -9.8 dBc with a limiting amplifier. The loss of fundamental power due to parasitic spurs actually becomes quite negligible after limiting. For example, a 3 dB spur after limiting reduces the fundamental power by less than 1.4 dB.

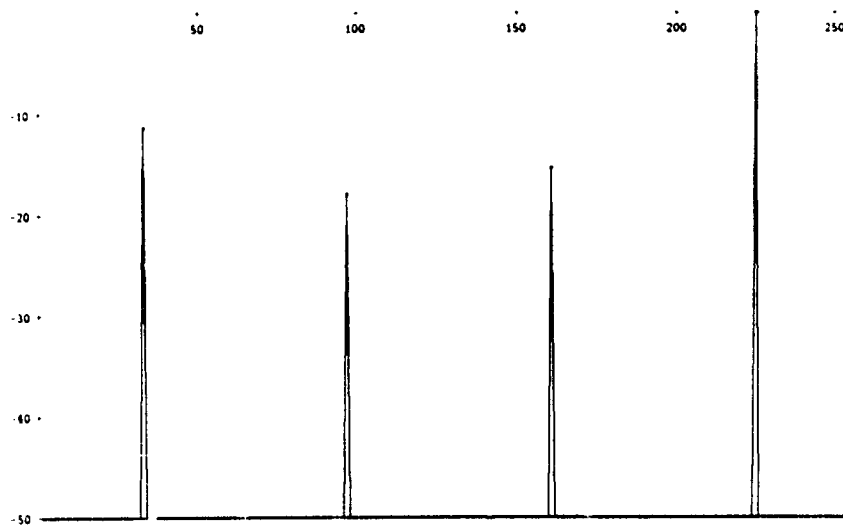
The calculations did not use random frequencies because rational divisors of 2π produce exact results using an FFT, providing an integer number of cycles are represented. Using 1/32 clock frequency increments produced uniform coverage of the DRFMU bandwidth and contained the frequencies where most of the aliased odd harmonics coexisted at discrete frequencies. For example, consider the two-state DRFMU (Table 1). The largest relative timing error exists at a frequency of 3/8 of the clock frequency, resulting in the maximum spur condition. This occurs because measured phase changes every 1.5 clock cycles, and the stored phase is either one or two clock cycles. These establish the maximum 33% error. Also, this is the single frequency where all the aliased odd harmonics coexist.

Figure 5 illustrates the spectra when spurs converge for an eight-state DRFMU. These are amplitude vs frequency plots for three different input frequencies. The frequency scale is again normalized to the clock. Figure 5(b) shows convergence at approximately 7/16 clock. Figures 5(a) and 5(c) are at very small increments of frequency below and above this point. These two plots are only close approximations to the theoretical frequencies since an integer number of cycles could not be used for the FFT.

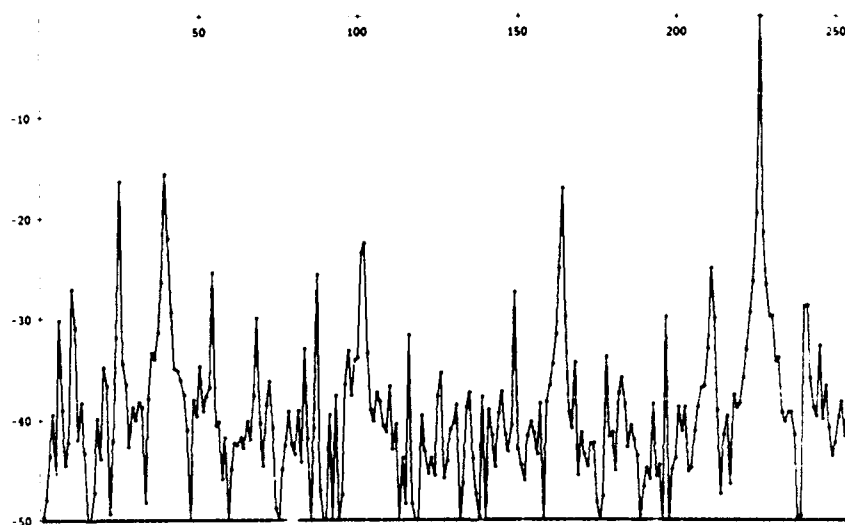
The results reveal no differences between the spurious performance of the two-state and four-state DRFMUs. For this reason, most manufacturers that make I/Q (four-state sampling) DRFMUs do not recombine I and Q before upconversion. This is because the increased hardware does not significantly enhance spurious performance. The I/Q sampling does, however, allow quadrature mixing, which doubles the available bandwidth and allows 90° phase modulation of the output signal. These two benefits more than offset the increased complexity and cost of the input stage plus additional memory.



(a) Spectrum display with fundamental frequency $< 7/16$ clock



(b) Spectrum with fundamental frequency $= 7/16$ clock



(c) Spectrum with fundamental frequency $> 7/16$ clock

Fig. 5 — Spurious signals converging to discrete frequencies

SIMULTANEOUS SIGNALS

Potential users of the phase DRFMU are also concerned about its response to simultaneous signals. Typically, ECM systems only respond to the strongest signal. However, laboratory and simulation subsystems may need to preserve the integrity of both signals. The phase DRFMU satisfies both demands. It responds to the strongest signal because of the limiting aspect of sampling. Additionally, it preserves the weaker signal. The relationship between the two signals is not linear but depends on the signals' relative location in frequency.

The theoretical response of a phase DRFMU to simultaneous signals was analyzed using the model shown in Fig. 6. The first step was to add the respective in-phase, quadrature phase, and 45° phase components of the two signals in floating point arithmetic. The next step was sampling both signals for an integer number of samples and quantizing the phase based on the I , Q , $I45$, and $Q45$ values. The resulting waveforms were unweighted for the eight-state DRFMU ($\pi/4$ radians is 0.5 times the voltage of $\pi/2$ radians instead of 0.707).

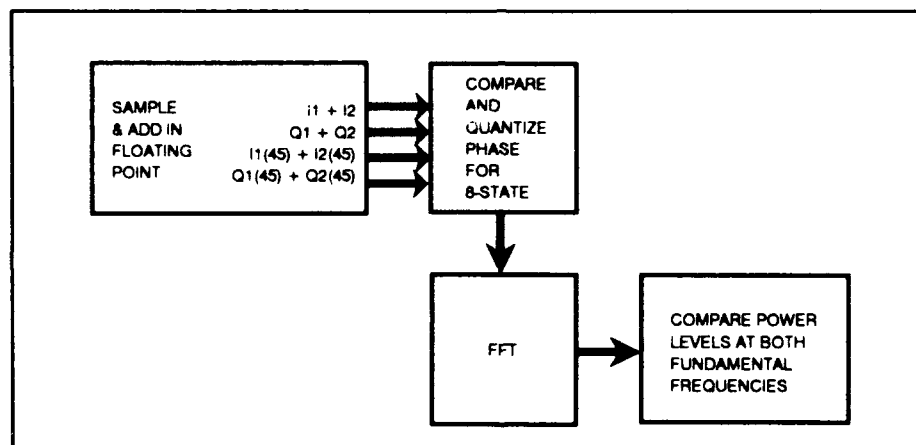


Fig. 6 — Process for analyzing simultaneous signals

Studying the results for both the eight-state and two-state sampling shows that the phase DRFMU generally favors the lower frequencies. This is because phase sampling causes the fundamental power to roll off as a function of frequency. Tables 6 and 7 show selected results for a two-state and an eight-state DRFMU. These contain values for the amplitude difference between two simultaneous signals at different frequencies. As in the spurious analysis, these tables do not represent an exhaustive study, rather they give the reader some understanding of two-state and eight-state phase DRFMU responses.

OUTPUT SIGNAL PHASE MODULATION

One major benefit from the phase DRFMU is that the user can modulate the phase of the output signal directly. The quantization of phase steps depends on the number of states of the DRFMU. For example, an eight-state phase DRFMU can modulate the output signal in increments of $\pi/4$ radians, while a four-state unit can modulate in increments of $\pi/2$ radians.

The method for modulating the phase is straightforward in a four-state DRFMU and is accomplished by the appropriate rotations of I , Q , I' , and Q' as shown in Fig. 7. These depict four typical signal outputs in phasor notation, first with no phase shift, and then with three sequential 90° shifts. The table in the figure shows the logic state diagram for the complete range of phase shifts obtainable. A barrel shifter rotates the phase of the inputs I , Q , I' , and Q' in response to two control inputs (four rotations).

Table 6 — Difference in Output Signals for
Eight-State DRFMU with Two Inputs

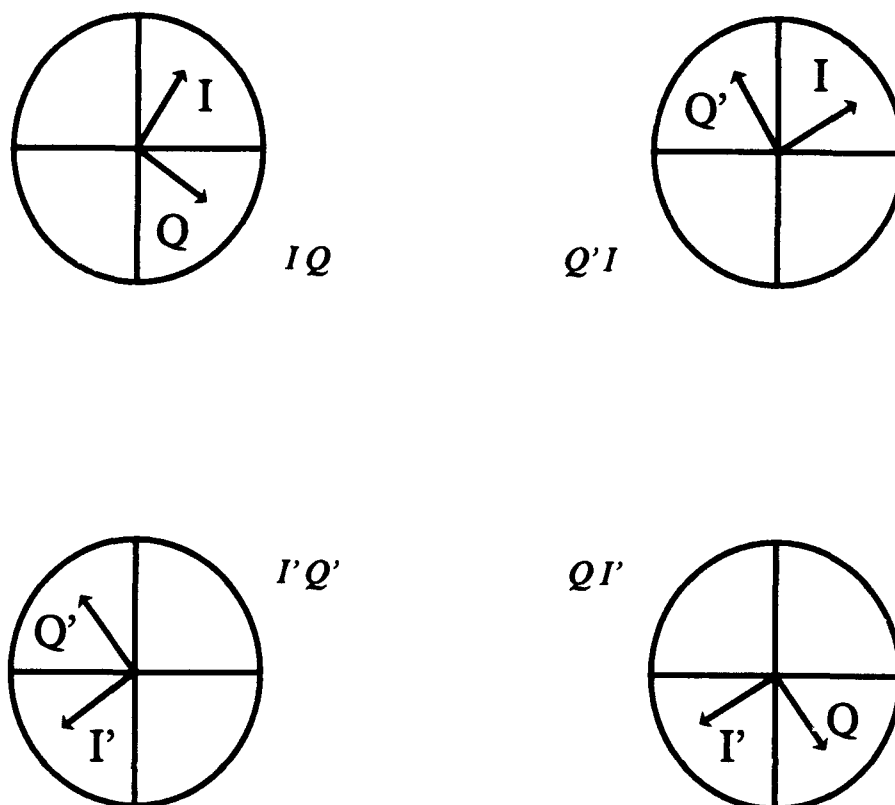
Voltage Ratio f_1/f_2	Output Power Ratio (dB)			
	Set 1		Set 2	
	f_1 1/16	f_2 1/4	f_1 3/32	f_2 9/32
1.0	-0.4	0	0.6	0
0.707	-2.8	1.0	-2.0	1.6
0.50	-3.6	1.4	-2.8	1.5
0.25	-3.1	1.7	-6.7	2.0
0.125	-5.8	2.0	-6.0	1.8

- f_1 and f_2 are ratios of the clock frequency
- Output power is referenced to f_2 level for input ratio = 1

Table 7 — Power Difference
Between Two Simultaneous Signals in a
Two-state DRFMU

Voltage Ratio f_1/f_2	Output Power Ratio (dB)			
	Set 1		Set 2	
	f_1 1/16	f_2 1/4	f_1 3/32	f_2 9/32
1.0	2.7	0	0.7	0
0.707	0.7	1.8	-1.4	1.4
0.50	-3.4	3.2	-3.1	1.8
0.25	-∞	3.2	-7.0	2.1
0.125	—	—	-10.2	2.1

- f_1 and f_2 are ratios of the clock frequency
- Output power is referenced to f_2 level for input ratio = 1



Input Signal Phase		Output Logic States			
		I	Q	Q'	I'
0	90	1	0	1	1
90	180	1	1	0	1
180	270	0	1	0	0
270	0	0	0	1	0
		I'	Q'	Q	I'
90	90	0	1	0	0
180	180	0	0	1	0
270	270	1	0	1	1
0	0	1	1	0	1

Fig. 7 — DRFMU output shifted in 90° increments

Control of an eight-state DRFMU requires more effort since a Johnson code adder is needed to offset the phase appropriately. This adder could either be hardwired or implemented as lookup tables that supply the desired phase increment (decrement) control to the phase shifter.

A phase correction can be applied to a recirculating signal by modulating the phase of the output signal. This capability can be very useful when recreating a longer replica from a captured signal containing only a small sample of the input. Phase correction is also valuable when generating a CW output from a captured pulse signal. According to a Fourier analysis, if no phase correction is applied, only frequencies that are integer multiples of $1/\sigma$ (where σ is the loop length) can exist within the loop. By applying phase correction, frequencies at integer multiples $1/n\sigma$ (where n is the number of equally spaced phase states) can exist in the loop. These frequencies depend on the pulse width; specifically, on the phase mismatch between the start and end of the stored pulse. In one case, for a frequency that is exactly halfway between two adjacent modal lines, the phase mismatch will be π radians. Recirculating this pulse uncorrected causes a biphasic modulation at a rate of $1/\tau$, where τ is equal to the stored pulse width. This results in "suckout," where almost all of the energy is at the frequencies $f_0 \pm 1/2\tau$ (some of the energy is lost to modulation products) and no energy is present at the carrier frequency (f_0), which is the frequency of interest. Applying the appropriate phase correction can ease this problem. Comparing the first and the last-plus-1 sample (an extra sample is taken for the phase correction) derives the needed phase correction. This reduces the modal spacing by a factor of the number of states of the DRFMU. Compared to a noncorrected signal, an eight-state phase-corrected signal would have eight times the number of possible frequencies, assuming uniform state spacing.

ADVANTAGES AND DISADVANTAGES

In summary, the advantages of the phase DRFMU are

- large bandwidth,
- large input signal dynamic range with no AGC requirement, and
- capability for direct phase modulation.

The disadvantages are that, for an equivalent number of bits, the phase DRFMU has higher spurs than does an amplitude DRFMU. The number of comparisons that must be made sets the practical limitation on the number of states for a phase DRFMU. Obtaining the different phased signals becomes quite cumbersome after eight states. Also, any spurious analysis must consider the performance of the quadrature up-converter, since quadrature leakage can become the limiting factor.